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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,846	01/15/2004	John E. Barth JR.	FIS920030409US1	5081

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EXAMINER	
MAI, SON LUU	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,846	BARTH ET AL.	
	Examiner	Art Unit	
	Son L. Mai	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-8,13,14 and 17-19* is/are rejected.

7)☒ Claim(s) *9-12,15 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The Amendment filed 04-12-05 has been entered. Accordingly, claims 1-4, 6-19 are pending in the application.

Claim Objections

2. Claim 8 is objected to because of the following informalities: "second word addresses" (line 5) should read –second word address--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 13 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As to claim 13, the claim recites the limitations "said refresh bank select signal" (lines 1-2) and "said memory access bank select signal" (line 2). There are insufficient antecedent bases for these limitations in the claim. Perhaps, the Applicants refer to "a refresh command" and "bank select signal" in claim 1.

As to claim 19, it appears "a first bank select signal" (line 8) is the same as the first signal in line 5 and should read –the first bank select signal--. Secondly, "said memory array" (line 8) lacks antecedent basis. It is not clear which one of the memory

arrays is being referred to. Thirdly, it appears "a second bank select signal" (line 11) is the same as the second signal in line 5 and should read –the second bank select signal--. Fourthly, "said second memory" (line 12) lacks antecedent basis. Should it read –said second memory array--? Fifthly, "a memory refresh operation" (line 12) and "a memory access operation" (lines 12-13) should read --the memory refresh operation-- and --the memory access operation—for referring to operations in lines 6 and 9.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-4, 6-8, 14 and 17-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Agata (U.S. Patent 6,563,757).

Regarding claim 1, Agata discloses a semiconductor memory (figure 6) comprising: a plurality of memory arrays (11), each of which comprises a plurality of memory cells arranged in a matrix and controlled by a row address counter (61) uniquely assigned to each of said memory arrays, said row address counter generating a first word address (refresh address; column 6, lines 58-62); and means (13) for enabling a refresh operation in said memory cells, said memory cells being identified by

said first word address when a refresh command (CLKref) is issued to a corresponding memory array, and a memory access command (column 4, line 56 through column 5, line 17) is provided by a bank select signal (from control circuit 13 to selector 31) to a corresponding memory array.

Regarding claim 2, Agata further teaches each of said memory arrays further comprises a second word address (row address from ROW PREDECODER 16) common to at least two of said memory arrays, and wherein an enabling means (13) enables a memory access operation (read or write) in said memory cells, said memory cells being identified by said second word address when a memory access command is issued to a corresponding memory array (column 4, lines 51-67).

Regarding claim 3, Agata teaches the refresh command is provided by a refresh bank select signal (CLKref) to a corresponding memory array.

Regarding claim 4, Agata teaches the first word address is updated when said refresh operation has been completed, by incrementing said row address counter (column 6, lines 58-62).

Regarding claim 6, Agata teaches said refresh bank select signal enables a refresh operation in said first memory array while concurrently enabling a memory access operation (read or write operation) in said second memory array (column 4, line 56 through column 5, line 25).

Regarding claim 7, Agata teaches said refresh bank select signal enables a refresh operation in at least one additional memory array while concurrently enabling a

memory refresh operation in said first memory array and a memory access operation in said second memory array (column 4, line 56 through column 5, line 25).

Regarding claim 8, Agata teaches each of said plurality of the memory arrays further comprises switching means (SELECTOR 31) for selectively coupling said first and said second word address to row decoders within said memory array, and wherein a refresh operation is controlled by said first word address, and a memory access operation is controlled by the second word addresses.

Regarding claim 14, Agata teaches the refresh bank and the memory access bank are distinct from each other (column 5, lines 3-17).

Regarding claim 17, Agata teaches a semiconductor memory device (figure 6) comprising: a plurality of memory arrays (11), each of said memory arrays comprising a plurality of memory cells arranged in a matrix and controlled by a row address counter (61) uniquely assigned to each of said each memory arrays, said row address counter generating a first word address (refresh address; column 6, lines 58-62); means (13) enabling a refresh operation in said memory cells, wherein said memory cells are identified by the first word address when a refresh command (CLKref) is provided to a corresponding memory array; a common second address (row address from row predecoder 16) coupling at least two memory arrays; means (31) for selectively coupling said first and said second word addresses to row decoders within each of said memory arrays, wherein a refresh operation is enabled by said first word address in a first memory array while enabling a memory access operation by said second word address in a second memory array (column 5, lines 2-59).

Regarding claim 18, Agata teaches the first word address is updated when said refresh operation has been completed, by incrementing said row address counter (column 6, lines 58-62).

Regarding claim 19, Agata teaches a semiconductor memory (figure 6) comprising: a plurality of memory arrays (11), each of which comprises a plurality of memory cells arranged in a matrix and controlled by a row address counter (61) uniquely assigned to each of said memory array, said row address counter generating a first word address (refresh address; column 6, lines 58-62); first and second bank select signals (from control circuit 13 to selector 31) coupled to each of said memory arrays; means (13) for enabling a refresh operation for first memory cells in a first memory array of said memory arrays, said first memory cells being identified by said first word address when a refresh command is provided by a first bank select signal (from control circuit 13 to selector 31) to said memory array (column 5, lines 3-17); and means (13) for enabling a memory access operation for second memory cells in a second memory array of said memory arrays, said second memory cells being identified by a second word address (row address from ROW PREDECODER 16) when a memory access command is provided by a second bank select signal (from control circuit 13 to selector 31) to said second memory wherein a memory refresh operation in said first memory array and a memory access operation in said second memory array are concurrently enabled (column 4, lines 56 through column 5, line 17).

Allowable Subject Matter

7. Claims 9-12, 15-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claim 13 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach the further limitation of claim 9 wherein each of the memory arrays further comprising word address latches. The word address latches are coupled to the switching means, and wherein a third memory array initiates a memory access operation when the corresponding bank select signal is provided to the third memory array without waiting for the completion of: the refresh operation in the first memory array, and the memory access operation in the second memory array.

Response to Arguments

10. Applicant's arguments filed 04-12-05 have been fully considered but they are not persuasive. The amended claim 1 does not include all the limitations of claims 2, 3 and 5 as suggested in the previous Office action; therefore claim 1 and 2-4, 6-8 are rejected as being anticipated by Agata. The rejections of claims 17 and 18 stated in the previous Office action are repeated here. The rejection of newly presented claim 19 is set forth above.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son L. Mai whose telephone number is 571-272-1786. The examiner can normally be reached on 8am to 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

07-07-05

Son L. Mai
Primary Examiner
Art Unit 2827